

Overcome Forward Error Correction Challenges in 400G Device Designs

As data rates increase, so do the challenges of device design, validation, and test. The use of 4-level pulse amplitude modulation (PAM4) signaling has changed Ethernet test requirements. Due to the reduced signal to noise ratio (SNR), PAM4 links do not necessarily run error-free and require forward error correction (FEC). FEC is an advanced coding technique that sends the required information to correct errors through the link along with the payload data. The benefit of “forward” in FEC is that there is no need to retransmit information to correct errors detected at the receiver.

FEC is especially beneficial in applications where retransmissions are costly or impossible, such as one-way communication links and transitions to multiple receivers in data centers. The FEC technique controls errors in data transmissions over unreliable or noisy channels. FEC transforms transmitted data (message sequences) into code words that include redundant data. The receiver decoder uses the added redundancy to detect, and possibly correct, errors that may occur in the message, minimizing the need to retransmit.



Highlights in this paper include:

- forward error correction (FEC) overview
- FEC basics for link testing
- physical layer FEC test challenges

FEC Basics for Link Testing

The PAM4 modulation scheme and FEC technique enable data transmissions of 400 gigabits per second (Gb/s) and higher. Specifications for all 400 gigabit Ethernet (GE) systems now require FEC. The Institute of Electrical and Electronics Engineers (IEEE) standard for 100GE backplane first defined the RS(544, 514) or KP4 and RS(544, 528) or KR4 FEC Reed-Solomon codes for Ethernet test. Reed-Solomon codes use symbols and codewords rather than bytes and frames to correct symbol errors rather than bit errors. Note that in the case of FEC, the term “symbol” does not equate to PAM4 symbols. All RS FEC decoding is done at the bit level after the conversion of the PAM4 gray code to a non-return-to-zero (NRZ) bitstream.

Before FEC, engineers tested signal transmissions by checking for packet errors to ensure that the bit error ratio (BER) was better than 10^{-12} (or 10^{-15} depending on the interface). However, even with the use of FEC, engineers must still check for BER and bit errors. Figure 1 shows the new FEC measurements, such as frame loss rates (FLR) and codewords, required to verify the transmission link. FLR, a ratio of lost packets to the total number of packets, is a new IEEE metric for uncorrectable code words in high-speed Ethernet links with FEC. Since errors are pro-actively corrected, it is less obvious whether the transmissions are “good”, and engineers must take a closer look at the transmission trends.

FEC Statistics

- Per lane and aggregate across lanes
 - “Pre FEC” total bit errors & BER (10^{-4} to 10^{-6})
 - “Pre FEC” symbol error count & symbol error rate
- FEC frame loss rates (FLR) (10^{-12} or 10^{-15} depending on the interface)
- Codewords (corrected, uncorrectable, total)
- FEC max corrected symbols
- Symbol error distribution

Figure 1. FEC statistics to verify 400 Gb/s transmission

Physical Layer FEC Test Challenges

Data striping is often used to lower the incidents of frame losses in links employing multiple lanes operating at a sub-rate of the total link data rate. Striping the data rotates the individual data streams through all the available lanes in the link in a round-robin fashion. By striping, burst errors generated by pass-through re-timers within the link will have the length of any error burst effectively divided by the number of lanes used for the striping. For example, in a 100GE link using four lanes of 25.78 Gb/s NRZ data, an error burst of 100 bits generated in an optical module on a single lane would result in only 25 errors on that single lane after deinterleaving striping at the end of the link. Therefore, while striping does not increase the computed coding gain, which assumes random error distribution, it effectively increases the gain when error bursts occur.

A 400GE test provides FEC statistics striped over all lanes and includes bit errors, BER, and FEC symbol error ratio (SER). This information is crucial to help identify problems. Even though the FEC statistics show all acceptable results, problems with the transmission are still possible. For example, the pre-FEC symbol error distribution can be high with a low passing margin, which is not acceptable.

Figure 2 shows an example where the FLR is below 10^{-10} , and the pre-FEC BER is better than -4 , indicating this system has passed the test. In this case, a frame refers to an Ethernet frame. A closer look at the results shows up to 15 errors per codeword, indicating an unhealthy link since the link has no margin as KP4 FEC cannot correct more than 15 errors per frame. It is important to identify and correct the source of errors for this device. Engineers need to understand FEC test implications and look deeper into test results to achieve a healthy system.



FEC Total Bit Errors	1,685,086,529
FEC Max Corrected Symbols	15
FEC Corrected Codewords	787,415,758
FEC Total Codewords	8,747,730,910
FEC Frame Loss Ratio	0.00e+000
pre FEC Bit Error Rate	3.54e-005
FEC Codeword with 0 error	7,960,315,152
FEC Codeword with 1 error	551,108,911
FEC Codeword with 2 errors	200,069,411
FEC Codeword with 3 errors	26,209,344
FEC Codeword with 4 errors	8,176,726
FEC Codeword with 5 errors	1,363,216
FEC Codeword with 6 errors	382,557
FEC Codeword with 7 errors	77,640
FEC Codeword with 8 errors	21,150
FEC Codeword with 9 errors	4,968
FEC Codeword with 10 errors	1,349
FEC Codeword with 11 errors	356
FEC Codeword with 12 errors	93
FEC Codeword with 13 errors	26
FEC Codeword with 14 errors	8
FEC Codeword with 15 errors	3
FEC Uncorrectable Codewords	0



Figure 2. Example of FEC testing

System tests need to change as new measurements are required to support 400G, PAM4, and FEC. The key measurements affected by FEC test implications include the transmitter (output) and receiver (input) burst error counting and analysis. Testing with stressed FEC-encoded data and measuring BER in links that do not by design run error-free is also important.

Transmitters

The FEC coding mechanism does not affect the transmitter itself. For example, transmitter measurements such as eye height and jitter will not change whether the data is FEC encoded or not. However, a reference receiver is required to perform these measurements. When implemented in a sampling scope, the precision filters in a reference receiver require the scope to pattern lock on the test pattern. Sampling scopes have a maximum pattern length limit of 2^{16} bits to achieve pattern lock. The pattern length of FEC-encoded data will exceed this limit.

Receiver

Since the receiver decoder is responsible for detecting the added redundancy in transmitted data and correct message errors, the test requirements for receivers are more extensive. You need to detect and process all eight electrical tributaries of the 400GAUI-8 interface to decode the FEC encoding and measure FLR. New receiver tests include burst error counting (FLR) and analysis, testing with stressed FEC-encoded data, and BER measurement in links.

Burst error counting requirements

In receivers, a BER measurement of less than 2.4×10^{-4} is required to meet the 400G class Ethernet standard IEEE 802.3 (see Figure 3). Designers need access to FEC engine statistics to detect burst errors that cause the Reed-Solomon decoder to fail due to an excessive number of correctable errors per codeword. Decision feedback equalizers (DFE) can open PAM4 eyes but are known to propagate errors. As a result, more than acceptable correctable errors per codeword can occur in links when using a DFE. It only takes a couple of errors to result in a burst of output errors that overload the Reed-Solomon decoder. The only way to discover them is by testing beyond BER.

The best way to test burst errors is to transmit a test pattern, as if from an FEC encoder. The device under test's (DUT) FEC decoder counts the Reed-Solomon decoder failures or the number of lost frames. The number of lost frames compared to the total number of frames provides the FLR value. For this test setup, it is important to ensure that the FEC encoder provides the proper pattern for testing.

122.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 120 shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.233) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

Figure 3. Bit error ratio clause in the IEEE 802.3 clause 122 (400GBASE-FR8/400GBASE-LR8)

Receiver test with stressed FEC encoded data

Typically, classical jitter and sensitivity tolerance tests use pseudo-random binary sequence (PRBS) patterns. However, it is also possible to use FEC encoded data for access to FEC statistics. One approach uses a compliant DUT transmitter as the pattern generator (see Figure 4). In this approach, the DUT handles the complex FEC encoding. Generate stress by applying a jitter clock to the Tx clock input. Calculating the calibrated stress is a challenge because the eye closure scales depending on the clock multiplier factor. It takes multiple test iterations to determine the stress test levels. However, there is a significant challenge using this technique. The resulting test determines a pass/fail of compliance status but not for margin tests. Margin tests require the stress to increase to the point of failure to determine the margin, but the clock input's re-clocker strips the high-frequency stress.

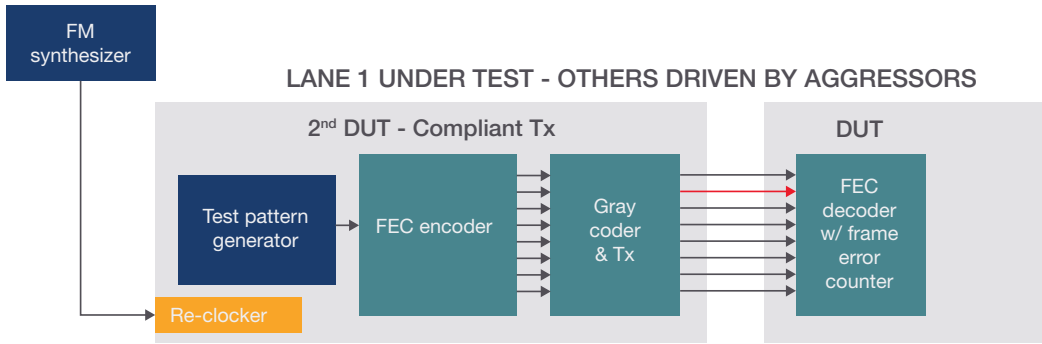


Figure 4. BERT pattern generator with FEC encoding

Most users prefer to use a BERT to alleviate this problem. However, until recently, a BERT only solution did not provide the required FEC encoding to perform this test. Keysight's new solution combines a BERT to generate the stress lane under test with a protocol generator to provide the unstressed striped FEC-encoded lanes required to perform the test (see Figure 5).

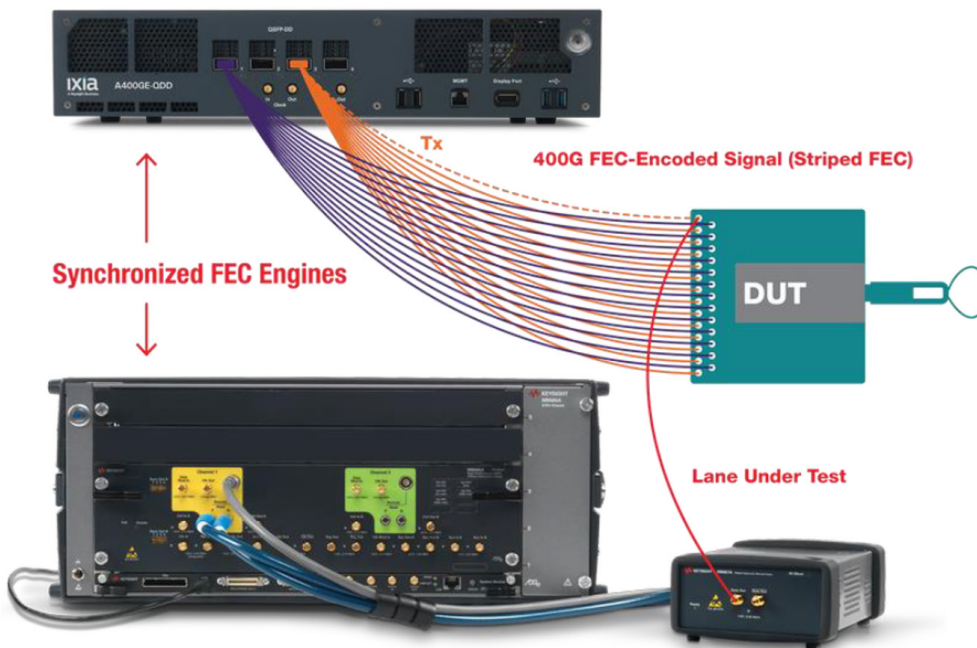


Figure 5. N4891A 400GBASE FEC-aware receiver test solution

Mandatory FEC-Aware Layer 1 Testing

The implementation of FEC in 400G devices eliminates errors in data center communications. Test standards for 400G and beyond require FEC in layer1 testing to characterize the system margin and to correct errors in data transmission that otherwise do not run error-free by design. FEC primarily affects device receiver testing, but there are transmitter test implications to consider as well. An understanding of FEC test implications will save time and help achieve optimal results.

Engineers need to overcome test challenges introduced by FEC such as new:

- 400G design requirements (ex. avoid burst error mechanisms)
- metrics such as FLR and FEC margin

Using the recommended Keysight instruments and software will help you achieve successful 400G device test results.

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